USB - CyberCl

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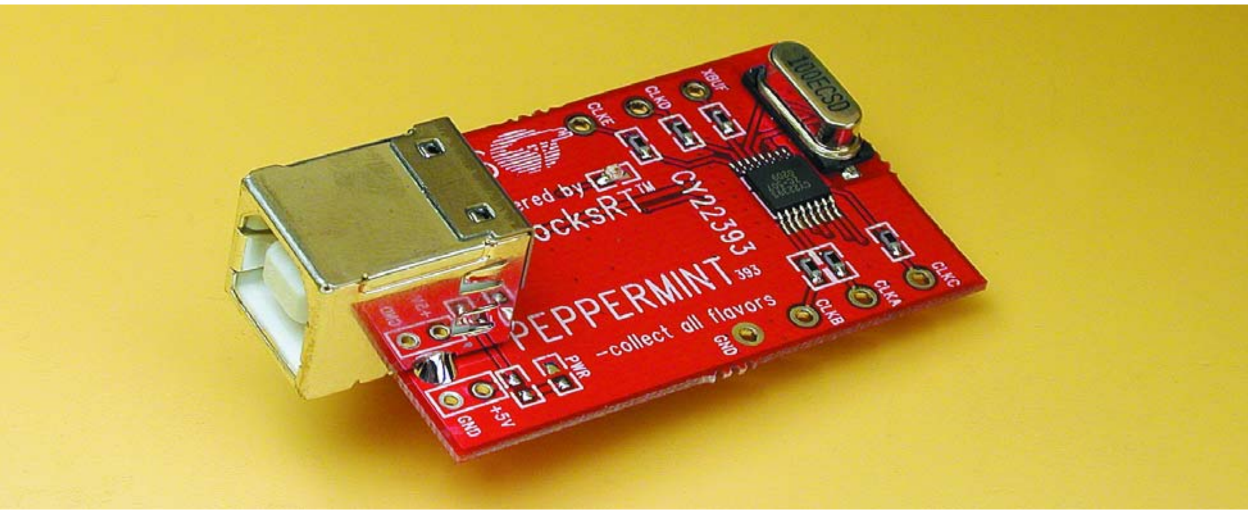

Quartz oscillators are the way to go when you need a precise, stable frequency source but what do you do when an application calls for a non-standard frequency? Custom-made crystals are an expensive option but now Cypress has come up with a cheaper alternative…

The buzzword is CyberClock and describes a relatively new technology in the field of clock generators for use in complex systems like PC motherboards. If you take a look at an old motherboard it is easy to spot the crystal generators dotted around the board providing all the different clock sources. More modern systems are increasingly employing just a single clock generator and deriving all the other signals from this one source.

PLL Technology

The clock generator chips contain a Phase Locked Loop (PLL) with the fastest versions having an output frequency range from 100 MHz to 400 MHz. The PLL layout is shown in **Figure 1.** It differs from a standard PLL by having programmable dividers at the input and output and in the feedback path. The input clock F_{REF} (typically a crystal) is connected to a programmable divider Q. This clock signal is now compared in the Phase Detector (PD) with the output frequency from the Voltage Controlled Oscillator (VCO) divided by P and fed to the Charge Pump (CP). The CP output is a function of the phase difference and controls the VCO. The VCO output is passed through the output divider *N* to produce F_{OUT}. Altogether there are three dividers (*Q*, *P* and *N*) all of which can be independently programmed.

We shall take a closer look at two of the Cypress clock chips. Firstly the CY22393 ('Three-PLL Serial Programmable, Flash Programmable Clock Generator') has six configurable outputs (**Figure 2**). The device can be flash-programmed (non volatile) from a special external programmer. The programming algorithm is not in the public domain presumably for licence protection and to guard against over-clocking or similar abuse. While the oscillator is running it is possible for the contents of internal registers can be overwritten via the I^{2}C-Bus but this storage is volatile and they will be lost on power down.

The CY27EE16 ('One-PLL In-System Programmable Clock Generator with Individual 16K EEPROM') is particularly interesting for low volume production applications or circuit development. The internal EEPROM does not need a special programmer; it can be programmed via the built-in I^{2}C bus interface. Register contents can also be overwritten 'on the fly' as above. A default configuration can be programmed into the chip and this will be loaded each time at power up. This facility brings the concept of an individually programmable oscillator one step closer. The internal structure of the chip (**Figure 3)** shows the

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For low-noise VCOs & PLLs

possibilities for clock generation using just one PLL. The output dividers can be internally connected to either the VCO output or directly from the reference clock. One frequency can be freely chosen while the other outputs must be derived from the VCO or reference frequency.

Both ICs allow direct connection of a crystal in the range between 8 MHz and 30 MHz. The output frequency is selectable up to 200 MHz.

A range of evaluation boards from Cypress featuring USB connectivity supports the family of clock generator chips. These boards are known as ‘Candy Boards’ (presumably because they are simple to use). The ‘Peppermint board’ has the CY22393 fitted while the ‘Blueberry board’ contains the CY27EE16. Each of these evaluation boards is a versatile stand-alone universal frequency generator and can be used in many applications. CyberClocks (**Figure 4**) is a free program that greatly simplifies the process of directly programming and controlling the Candy Boards.

Cypress also produces free downloadable software supporting the entire range of clock generators. From the CyberClock start menu select the sub-family then the chip part number. The CY22393 can be found under CyClocksRT while the CY27EE16 is under ISR.

The program displays a window for the selected chip with the programming options. The desired output frequency and the input clock frequency can be entered along with the pin-out configuration and the software will calculate the division factors *Q*, *P* and *N* and also all the necessary internal register values. The settings can be saved in a JEDEC format file that is compatible with most hardware programmers. The starter boards also feature a USB interface.

The Peppermint Board

The demo board type CY30701 (Peppermint Board) is fitted with the CY22393 and contains an on-board 10 MHz crystal together with a USB interface. The CyberClocks program can be used to configure the chip once the desired output frequencies are entered.

The example in **Figure 5** shows the generation of three different frequencies in the range between 6.55 MHz and 122 MHz. A buffered output clock from the quartz oscillator is also used as an output. With the software in *Advanced Mode* it is possible to see all the configuration settings. Details of each of the PLL and divider settings as well as all the internal links are shown. Another program feature that proved useful during system development is the *Bit-Viewer*, this displays the contents of all the internal registers.

When the Peppermint board is first connected to the PC it should be automatically detected and the appropriate Human Interface Device (HID) driver will be loaded by Windows. An on-board status LED will blink to indicate successful USB communication.

The board takes its power directly from the +5 V USB and has an on-board 3.3 V voltage regulator. Programmed settings will be retained on the board as long as it is powered up. Once power is disconnected the settings will revert to their default example values.

The Blueberry Board

For use in the lab the Blueberry Board (CY30703) with the CY27EE16 is particularly interesting. The double ‘E’ in the part number gives away the fact that the chip contains an EEPROM. This has space to store 2 kbits for reg-

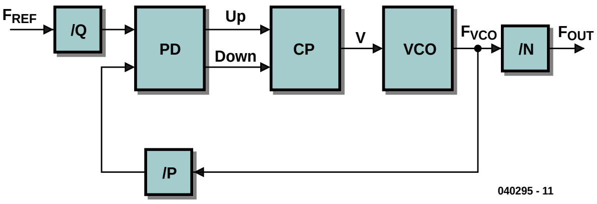


Figure 1. The PLL principle with feedback divider.

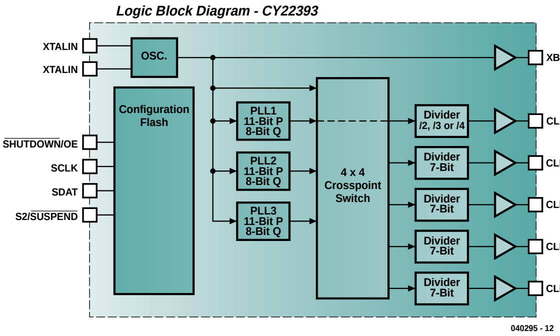


Figure 2. The CY22393 block diagram.

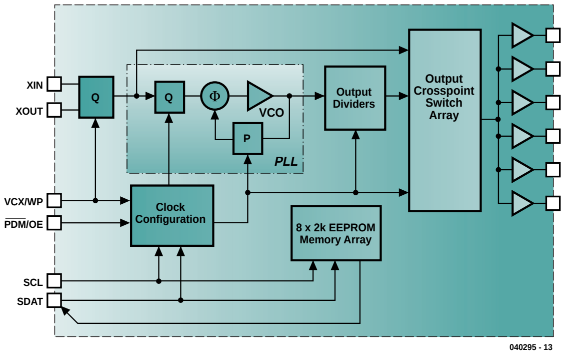


Figure 3. The CY27EE16 PLL and divider.

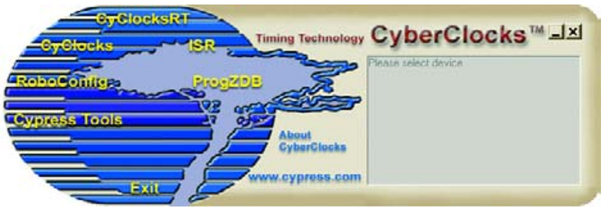
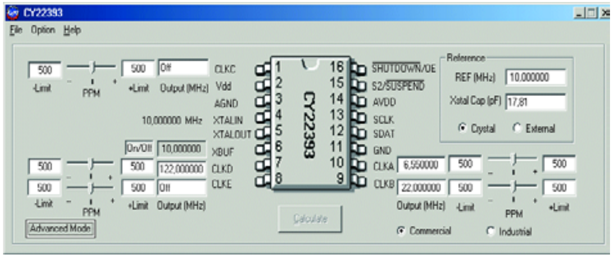


Figure 4. The CyberClocks programming tool.

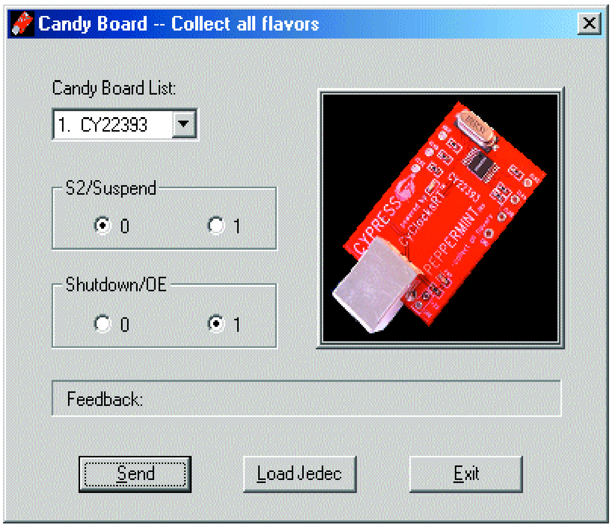
ister contents and a further 16 kbits for general program use. No special hardware is necessary to program the device. The clock configuration parameters can be stored either in RAM or EEPROM. Storing to RAM allows the clock to be configured 'on the fly'. After a power down/up cycle the clock will be reconfigured to the parameters stored in EEPROM.

This chip has only one internal PLL but with careful programming of the dividers many different clock frequencies can be generated. To increase flexibility the output dividers can be switched to either the PLL output or to the oscillator frequency and an output crosspoint switch matrix routes the clocks to the user defined output pins.



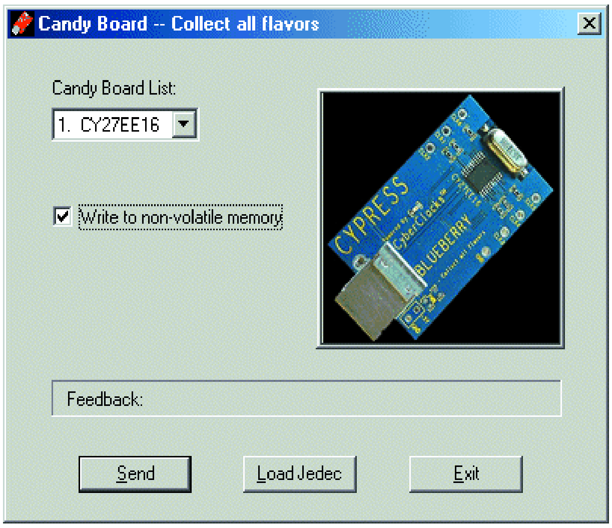
REF (MHz) 10.000000
Xtal Cap (pF) 17,81
● Crystal ○ External
CLKC: 500 -Limit, 500 +Limit, Output (MHz) Off
XTALIN: 10,000000 MHz
XBUF: 10,000000
CLKD: 500 -Limit, 500 +Limit, Output (MHz) 122,000000
CLKE: 500 -Limit, 500 +Limit, Output (MHz) Off
CLKA: Output (MHz) 6,550000, 500 -Limit, 500 +Limit
CLKB: Output (MHz) 22,000000, 500 -Limit, 500 +Limit
● Commercial ○ Industrial

Figure 5. Frequency selection on the peppermint board.



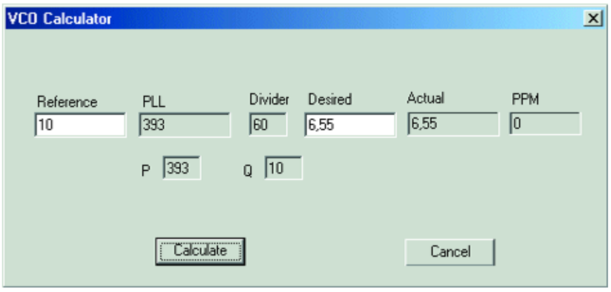
Candy Board List: 1. CY22393
S2/Suspend: ● 0 ○ 1
Shutdown/OE: ○ 0 ● 1
Feedback:

Figure 6. USB data transfer.



Candy Board List: 1. CY27EE16
☑ Write to non-volatile memory
Feedback:

Figure 7. Programming the settings into EEPROM.



Reference 10
PLL 393
Divider 60
Desired 6,55
Actual 6,55
PPM 0
P 393
Q 10

Figure 8. Factors P, Q and N in the VCO calculator.

RF applications

These signal generators are essentially intended as clock sources for microprocessor systems and their peripherals but we are all in favour of a bit of experimentation so why shouldn't we try it out for RF applications? The main concern is whether the generator can meet the more stringent requirements of an RF environment. In particular the increased level of phase noise in a PLL system compared to a Direct Digital Synthesiser (DDS) could impact on a receiver's performance. The acid test would be to use it in place of the synthesised signal at the first injection oscillator input to the digital (DRM) receiver published in March 2004 of *Elektor Electronics*. For example, to receive DRM transmissions from the German station RTL (broadcasting on 6095 kHz) we require a first oscillator of 6550 kHz (with an IF of 455 kHz, 6095 + 455 = 6550 kHz). After substituting the PLL clock for the DDS clock the resulting performance was surprising good: The DRM signal was completely clean and indistinguishable from the quality achieved with the DDS clock source. Based on this result there seems to be no good reason why the programmable oscillator should not be considered for use in critical RF applications also.

Anyone who has worked with PLLs will be aware of the usual problems: A VCO is controlled by the output signal from a phase comparator and a loop filter, this configuration gives rise to relatively high levels of phase noise and the effects of loop resonance. In critical RF applications LC oscillators with high Q characteristics are used to reduce these tendencies but never the less PLL based receivers usually tend to have higher levels of phase noise than for example, DDS controlled receivers. The performance achieved here is therefore remarkably good.

The *VCO Calculator* in CyberClocks details how 6.550 MHz is derived from the 10 MHz clock. The *Q* divider is set to 4, giving a fairly high comparison frequency of 2.5 MHz. The PLL (the *P* divider) multiplies the frequency by a factor of 131 to produce 327.5 MHz. The VCO output is divided by 50 in the output dividers to give an output of: 10 MHz / 4 · 131 / 50 = 6.550 MHz.

The secret of the high quality signal lies in the fact that the VCO and comparison frequency are relatively high and the VCO phase noise on the output signal is effectively divided down by the output divider chain (*N*). By comparison a conventional PLL system with a channel spacing of 10 kHz would typically use a comparison frequency of 10 KHz with the output frequency sourced directly from the VCO output, this set-up makes it far more difficult to produce a clean signal.

The Blueberry board can generate signals higher than those produced by the DDS of the *Elektor Electronics* DRM receiver so it is now possible to explore the short wave region around 26 MHz. The receiver design uses a wideband first mixer stage connected directly to the aerial so it is also possible to push the oscillator frequency up a bit more and receive signals in the VHF band. It is perfectly possible to cover transmissions in the aircraft and 2 m amateur radio band; all we need now are some DRM stations up there to listen to.

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